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10/551,415	11/17/2005	Toshiyuki Oga	Q90624	4446
23373 7590 01/10/2008 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER NGUYEN, TUAN HOANG	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/551,415

Applicant(s)

OGA, TOSHIYUKI

Examiner

Tuan H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-50 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-10, and 13-50 is/are rejected.
- 7) ☒ Claim(s) 3,4,11 and 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response To Arguments*

1. Applicant's arguments filed on 10/26/2007 have been fully considered but they are not persuasive.

In response to Applicant's remark on pages 27-30, Applicant argues that Ono et al. (U.S PAT. 7,050,779 hereinafter, "Ono") reference cited by the Examiner does not disclose or suggest at least "wherein said baseband processing section and said information processing terminal operate in synchronization with a clock" (Applicant remarks on page 27). Examiner respectfully disagrees with the Applicant arguments. Applicant should refer to Ono reference (i.e., "a control register CRG is provided in the control circuit 27, and the setting of the register CRG is made on the basis of the signals from the baseband circuit 6. More concretely, clock signals CLK for synchronization, data signals SDATA, and load enable signals LEN as control signals are supplied to the RF processing unit 5 (information processing terminal) from the baseband circuit 6 (baseband processing section). When the load enable signals LEN are asserted to effective levels, the control circuit 27 sequentially takes in the data signals SDATA transmitted from the baseband circuit 6 in synchronization with the clock signals CLK to set them into the above-mentioned control register CRG", figure 1, col. 6 lines 18-28). where as the Examiner interpreted "wherein said baseband processing section and said information processing terminal operate in synchronization with a clock". Applicant also

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argues that “at least an information processing terminal which converts the reception digital baseband signal into a reception data and converts a transmission data into a transmission digital baseband signal” would not be obvious in light of Ono (Applicant remarks on page 28) and that “Ono, discloses an integrated circuit which provides only analog R\_F-to baseband conversion and analog baseband-to-RF conversion of the information signals. As disclosed by Ono, analog-to-digital conversion and digital-to-analog conversion is provided only for generating input offset voltages to the programmable gain amplifiers” (Applicant remarks on page 28). Examiner respectfully disagrees with the Applicant arguments. Applicant should refer to Ono reference (i.e., “the high-gain amplifier sections 13 and 14 respectively amplify the demodulated I and Q signals to output them to the baseband circuit 6”, col. 4 lines 29-31). Since, analog-to-digital conversion and digital-to-analog conversion is provided for generating input offset voltages to the programmable gain amplifiers. Thus, the reception signal should be a digital baseband signal input digital-to-analog conversion is provided to the programmable gain amplifiers to convert to the reception data and transmission data input to the analog-to-digital is provided to the programmable gain amplifiers to output to the digital baseband signal. Thus, the RF processing unit 5 (an information processing terminal) converts the reception digital baseband signal into a reception data and converts a transmission data into a transmission digital baseband signal. Therefore, the teaching of the prior art references still read on.

Base on the above rational, it is believed that the claimed limitations are met by the references submitted and therefore, the rejection maintained.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 9, 16-29, 39 and 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura Shigeru et al. (Japanese Publication Number: 08-149035 hereinafter, "Imura") in view of Ono et al. (U.S PAT. 7,050,779 hereinafter, "Ono").

Consider claims 1 and 21, Imura teaches an information processing terminal system comprising: an information processing terminal (page 3 [0029]); and a transmitting and receiving unit which can be attached to or detached from said information processing terminal (page 3 [0030]), wherein said transmitting and receiving unit comprises: a transmission and reception processing section; a demodulation section; a modulation section and a baseband processing section (page 2 [0018]-[0020]) and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to the network (page 3 [0026]), said demodulation section converts the

reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]).

Imura does not explicitly show that baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal, and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal, said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal; said baseband processing section and information processing terminal operate in synchronization with a clock, and the reception digital signal contains a reception data, and the transmission digital signal contains a transmission data.

In the same field of endeavor, Ono teaches baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal, and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal (col. 3 lines 54-60 and col. 4 lines 25-47), said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal (col. 3 lines 54-60); said baseband processing section and information processing terminal operate in synchronization with a clock (fig. 1 col. 6 lines 18-31), and the reception digital signal contains a reception data, and the transmission digital signal contains a transmission data (col. 3 lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal, and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal, said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal; said baseband processing section and information processing terminal operate in synchronization with a clock, and the reception digital signal contains a reception data, and the transmission digital signal contains a transmission data, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 2, Imura further teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal as the reception digital signal to output to said information processing terminal (page 3 [0021]); and converts a transmission digital baseband signal as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and

converts the transmission data into the transmission digital baseband signal (page 2 [0020]).

Consider claim 9, Imura further teaches said baseband processing section converts the reception analog baseband signal into the reception data as the reception digital signal to output to said information processing terminal and converts the transmission data as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020]) and page 3 [0021]).

Consider claim 16, Imura teaches information processing terminal system comprising: an information processing terminal (page 3 [0029]); and a transmitting and receiving unit which can be attached to and detached from said information processing terminal (page 3 [0030]), wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, a modulation section and a baseband processing section (page 2 [0018]-[0020] and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog



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baseband signal (page 3 [0020]), said baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal said modulation section converts the transmission analog baseband signal into a transmission modulation wave signal (page 3 [0020]).

Imura does not explicitly show that said baseband processing section and information processing terminal operate in synchronization with a clock; and information processing terminal converts the reception digital baseband signal from said baseband processing section into a reception data and converts a transmission data into the transmission digital baseband signal.

In the same field of endeavor, Ono teaches said baseband processing section and information processing terminal operate in synchronization with a clock (fig. 1 col. 6 lines 18-31); and information processing terminal converts the reception digital baseband signal from said baseband processing section into a reception data and converts a transmission data into the transmission digital baseband signal (col. 3 lines 54-60 and col. 4 lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, said baseband processing section and information processing terminal operate in synchronization with a clock; and information processing terminal converts the reception digital baseband signal from said baseband processing section into a reception data and converts a transmission data into the transmission digital baseband signal, as taught by Ono, in order to provide a semiconductor

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integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 17, Imura teaches a transmitting and receiving method in an information processing terminal system in which a detachable transmitting and receiving unit is attached to an information processing terminal, comprising:

(a) transmitting and receiving unit, demodulating a reception modulation wave signal from a network to convert into a reception analog baseband signal (page 2 [0020]) and page 3 [0021]).

Imura does not explicitly show that (b) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital signal containing a reception data in synchronization with a clock; (c) in said information processing terminal, receiving the reception digital signal in synchronization with the clock; (d) in said information processing terminal, sending a transmission digital signal containing a transmission data in synchronization with the clock; (e) in said transmitting and receiving unit, converting the transmission digital signal into a transmission analog baseband signal in synchronization with the clock; (f) in said transmitting and receiving unit, converting the transmission analog baseband signal into a transmission modulation wave signal; and (g) in said transmitting and receiving unit, transmitting the converted transmission modulation wave signal to the network.

In the same field of endeavor, Ono teaches (b) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital signal containing a reception data in synchronization with a clock (fig. 1 col. 6 lines 18-31); (c) in said information processing terminal, receiving the reception digital signal in synchronization with a clock (fig. 1 col. 6 lines 18-31); (d) in said information processing terminal, sending a transmission digital signal containing a transmission data in synchronization with the clock (fig. 1 col. 6 lines 18-31); (e) in said transmitting and receiving unit, converting the transmission digital signal into a transmission analog baseband signal in synchronization with the clock (fig. 1 col. 6 lines 18-31); (f) in said transmitting and receiving unit, converting the transmission analog baseband signal into a transmission modulation wave signal (col. 3 lines 54-60 and col. 4 lines 25-47); and (g) in said transmitting and receiving unit, transmitting the converted transmission modulation wave signal to the network (col. 3 lines 54-60 and col. 4 lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, (b) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital signal containing a reception data in synchronization with a clock; (c) in said information processing terminal, receiving the reception digital signal in synchronization with a clock; (d) in said information processing terminal, sending a transmission digital signal containing a transmission data in synchronization with the clock; (e) in said transmitting and receiving unit, converting the transmission digital signal into a transmission analog baseband signal in synchronization with the clock; (f) in said transmitting and

receiving unit, converting the transmission analog baseband signal into a transmission modulation wave signal; and (g) in said transmitting and receiving unit, transmitting the converted transmission modulation wave signal to the network, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 18, Imura further teaches wherein said (b) comprises (b1) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital baseband signal as the reception digital signal (page 2 [0020]), said (c) comprises (c1) in said information processing terminal, converting the reception digital baseband signal into the reception data (page 3 [0021]), said (d) comprises (d1) in said information processing terminal, converting the transmission data into a transmission digital baseband signal as the transmission digital signal (page 2 [0020]), and said (e) comprises (e1) in said transmitting and receiving unit, converting the transmission digital baseband signal into the transmission analog baseband signal (page 2 [0020]).

Consider claim 19, Imura further teaches wherein said (b) comprises (b2) in said transmitting and receiving unit, converting the reception analog baseband signal into the reception data as the reception digital signal, said (c) comprises (c2) in said information processing terminal, receiving the reception data (page 2 [0020]), said (d) comprises (d2) in said information processing terminal, outputting the transmission data as the

transmission digital signal to said transmitting and receiving unit (page 3 [0021]), and said (e) comprises (e2) in said transmitting and receiving unit, converting the transmission data into the transmission analog baseband signal (page 2 [0020]).

Consider claim 20, Imura teaches a transmitting and receiving method in an information processing terminal system in which a detachable transmitting and receiving unit is attached to an information processing terminal, comprising:

(h) in said transmitting and receiving unit, demodulating a reception modulation wave signal from a network to convert into a reception analog baseband signal (page 3 [0021]); (l) in said transmitting and receiving unit, converting the transmission digital baseband signal into a transmission analog baseband signal (page 2 [0020]); (m) in said transmitting and receiving unit, converting the transmission analog baseband signal into a transmission modulation wave signal (page 2 [0020]); and (n) in said transmitting and receiving unit, transmitting the transmission modulation wave signal to the network (page 3 [0026]).

Imura does not explicitly show that (i) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital baseband signal and in synchronization with a clock transmitting the reception digital baseband signal to said information processing terminal; and (j) in said information processing terminal, converting the reception digital baseband signal into a reception data in synchronization with the clock; (k) in said information processing terminal, converting a

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transmission data into a transmission digital baseband signal in synchronization with the clock.

In the same field of endeavor, Ono teaches (i) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital baseband signal and in synchronization with a clock transmitting the reception digital baseband signal to said information processing terminal (fig. 1 col. 6 lines 18-31) ; and (j) in said information processing terminal, converting the reception digital baseband signal into a reception data in synchronization with the clock; (k) in said information processing terminal, converting a transmission data into a transmission digital baseband signal in synchronization with the clock (col. 3 lines 54-60 and col. 4 lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, (i) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital baseband signal and in synchronization with a clock transmitting the reception digital baseband signal to said information processing terminal; and (j) in said information processing terminal, converting the reception digital baseband signal into a reception data; (k) in said information processing terminal, converting a transmission data into a transmission digital baseband signal, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 22, Imura further teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal as the reception digital signal to output to said information processing terminal, and converts a transmission digital baseband signal as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020] and page 3 [0021]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts the transmission data into the transmission digital baseband signal (page 2 [0020]).

Consider claim 23, Imura further teaches baseband processing section converts the reception analog baseband signal into the reception data as the reception digital signal to output to said information processing terminal, and the transmission data as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020] and page 3 [0021]).

Consider claim 24, Imura teaches an information processing terminal in an information processing terminal system comprising said information processing terminal and a transmitting and receiving unit which can be attached to or detached from said information processing terminal (page 3 [0030]), wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, a modulation section and a baseband processing section (page 2 [0020]), when

said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]).

Imura does not explicitly show that baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal, said modulation section converts the transmission analog baseband signal into a transmission modulation wave signal; said baseband processing section and said information processing terminal operate in synchronization with the clock, and the reception digital signal contains a reception data and the transmission digital signal contains a transmission data.

In the same field of endeavor, Ono teaches baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal (col. 3 lines 54-60 and col. 4 lines 25-47), said modulation section converts the transmission analog baseband signal into a transmission modulation wave signal (col. 3 lines 54-60 and col.



4 lines 25-47); said baseband processing section and said information processing terminal operate in synchronization with the clock (fig. 1 col. 6 lines 18-31), and the reception digital signal contains a reception data and the transmission digital signal contains a transmission data (col. 3 lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal, said modulation section converts the transmission analog baseband signal into a transmission modulation wave signal; said baseband processing section and said information processing terminal operate in synchronization with the clock, and the reception digital signal contains a reception data and the transmission digital signal contains a transmission data, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 25, Imura further teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal as the reception digital signal to output to said information processing terminal, and converts a transmission digital baseband signal as the transmission digital signal from said

information processing terminal into the transmission analog baseband signal (page 2 [0020] and page 3 [0021]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts the transmission data into the transmission digital baseband signal (page 2 [0020]).

Consider claim 26, Imura further teaches baseband processing section converts the reception analog baseband signal into the reception data as the reception digital signal to output to said information processing terminal (page 2 [0020]), and converts the transmission data as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 3 [0021]).

Consider claim 27, Imura teaches a transmitting and receiving unit in an information processing terminal system comprising an information processing terminal and said transmitting and receiving unit which can be attached to or detached from said information processing terminal, wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, an modulation section and a baseband processing section (page 2 [0020] and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said

network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]), and said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal (page 2 [0020]).

Imura does not explicitly show that baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal from said information processing terminal into a transmission analog baseband signal.

In the same field of endeavor, Ono teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal from said information processing terminal into a transmission analog baseband signal (col. 3 lines 54-60 and col. 4 lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal from said information processing terminal into a transmission analog baseband signal, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 28, Imura teaches an information processing terminal in an information processing terminal system comprising said information processing terminal and a transmitting and receiving unit which can be attached to or detached from said information processing terminal (page 2 [0020] and page 3 [0021]), wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, an modulation section and a baseband processing section (page 2 [0018]-[0020] and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]), said baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal from said information processing terminal into a transmission analog baseband signal (page 2 [0020]), said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal (page 2 [0020]).

Imura does not explicitly show that information processing terminal converts the reception digital baseband signal from said baseband processing section into the

reception data and converts a transmission data into the transmission digital baseband signal.

In the same field of endeavor, Ono teaches information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts a transmission data into the transmission digital baseband signal (col. 3 lines 54-60 and col. 4 lines 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts a transmission data into the transmission digital baseband signal, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 29, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit, wherein said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal (see fig. 10 page 2 [0016]).

Imura does not explicitly show that a clock generating circuit configured to generate a clock; and a first interface configured to operate in response to said clock, and said signal processing unit comprises: a second interface connected with said first

interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces.

In the same field of endeavor, Ono teaches a clock generating circuit configured to generate a clock (fig. 1 col. 6 line18-31); and a first interface configured to operate in response to said clock (col. 5 lines 52-61), and said signal processing unit comprises: a second interface connected with said first interface and configured to operate in response to said clock (fig. 1 col. 6 line18-31 and col. 6 line18-31); and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces (col. 3 lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, a clock generating circuit configured to generate a clock; and a first interface configured to operate in response to said clock, and said signal processing unit comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 39, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit (page 1 [0016]).

Imura does not explicitly show that signal processing unit comprises: a clock generating circuit configured to generate a clock; said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal; and a first interface configured to operate in response to said clock, and said signal processing unit further comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces.

In the same field of endeavor, Ono teaches signal processing unit comprises: a clock generating circuit configured to generate a clock (fig. 1 col. 6 line18-31); said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal (col. 3 lines 54-60); and a first interface configured to operate in response to said clock (col. 5 lines 52-61), and said signal processing unit further comprises: a second interface connected with said first interface and configured to operate in response to said clock (fig. 1 col. 6 line18-31 and col. 6 line18-31); and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces (col. 3 lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, signal processing unit comprises: a clock

generating circuit configured to generate a clock; said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal; and a first interface configured to operate in response to said clock, and said signal processing unit further comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 49, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit (see fig. 10 page 2 [0016]).

Imura does not explicitly show that radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; clock generating means for generating a clock; and first interface means for operating in response to said clock, and said signal processing unit comprises: second interface means connected with said first interface means for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interface means



In the same field of endeavor, Ono teaches radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal (col. 3 lines 54-60); clock generating means for generating a clock (col. 5 lines 52-61); and first interface means for operating in response to said clock (col. 5 lines 52-61), and said signal processing unit comprises: second interface means connected with said first interface means for operating in response to said clock (fig. 1 col. 6 line 18-31 and col. 6 line 18-31); and demodulation means for demodulating said reception digital signal supplied through said first and second interface means (col. 3 lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; clock generating means for generating a clock; and first interface means for operating in response to said clock, and said signal processing unit comprises: second interface means connected with said first interface means for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interface means, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

Consider claim 50, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit, (see fig. 10 page 2 [0016]).

Imura does not explicitly show that signal processing unit comprises: clock generating means for generating a clock, said radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; and first interface means for operating in response to said clock, and said signal processing unit further comprises: a second interface means connected with said first interface, for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interfaces.

In the same field of endeavor, Ono teaches signal processing unit comprises: clock generating means for generating a clock, said radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal (col. 3 lines 54-60 and col. 5 lines 52-61); and first interface means for operating in response to said clock (col. 5 lines 52-61), and said signal processing unit further comprises: a second interface means connected with said first interface, for operating in response to said clock (fig. 1 col. 6 line 18-31 and col. 6 line 18-31); and demodulation means for demodulating said reception digital signal supplied through said first and second interfaces (col. 3 lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, signal processing unit comprises: clock generating

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means for generating a clock, said radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; and first interface means for operating in response to said clock, and said signal processing unit further comprises: a second interface means connected with said first interface, for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interfaces, as taught by Ono, in order to provide a semiconductor integrated circuit device capable of largely improving the receiving sensitivity to the signals by reducing the thermal interference due to the self heating of each transistor constituting the gilbert cell circuit.

4. Claims 3, 6-8, 10, 13-15, 30-38 and 40-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura in view of Ono, and further in view of Philips et al. (U.S PUB. 2003/0118081 hereinafter, "Philips").

Consider claim 3, Imura and Ono, in combination, fails to teaches information processing terminal comprises: an interface; and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data and the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface, and said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said control unit as a clock.

However, Philips teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data and the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), and said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said control unit as a clock (page 4 [0046]).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Philips into view of Imura and Ono, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Consider claim 6, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data; and to convert the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 4 [0045]), said transmission and reception processing section generates and outputs a reference signal having a frequency to said clock generator (page 4 [0045]), said clock generator recovers a carrier of the reception

modulation wave signal based on the reference signal from said transmission and reception processing section to output to said demodulation section; and generates and outputs a reception symbol clock to said baseband processing section, said interface and said control unit as a clock (page 3 [0038]), said reception symbol clock is synchronous with the reference signal (page 3 [0035]), and said demodulation section, said baseband processing section, said interface and said control unit operate in synchronization with the reception symbol clock (page 3 [0035]).

Consider claims 7 and 14, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data (page 4 [0046]); and to convert the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claim 8, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data (page 4 [0045]); and a clock generator (page

3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claim 10, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), and said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said control unit as a clock (page 3 [0035]).

Consider claim 13, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section, and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), said transmission and reception processing section generates and outputs a reference signal having a frequency to said clock generator (page 4 [0045]), said clock generator recovers a carrier of the reception modulation wave signal based on the reference signal from said transmission and reception processing section to output to the demodulation section, and generates and outputs a reception symbol clock

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to said baseband processing section, said interface and said control unit as a clock (page 3 [0038]), said reception symbol clock is synchronous with the reference signal, and said demodulation section, said baseband processing section, said interface and the control unit operate in synchronization with the reception symbol clock (page 3 [0035]).

Consider claim 14, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section, and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claim 15, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section, and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to

output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claims 30 and 40, Imura and Ono, in combination, fails to teaches reception signal converting circuit operates in response to said clock.

However, Philips teaches reception signal converting circuit operates in response to said clock (page 3 [0035]).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Philips into view of Imura and Ono, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Consider claims 31 and 41, Philips further teaches demodulation section operates in response to said clock (page 3 [0038]).

Consider claims 32 and 42, Philips further teaches signal processing unit further comprises: a supply circuit configured to supply a transmission digital signal to said radio unit through said second interface (page 3 [0035]), and said radio unit further comprises: a transmission signal converting circuit configured to generate said a transmission radio signal from said transmission digital signal supplied through said first and second interfaces (page 8 [0130]).



Consider claims 33 and 43, Philips further teaches supply circuit operates in response to said clock (page 3 [0035]).

Consider claims 34 and 44, Philips further teaches transmission signal converting circuit operates in response to said clock (page 3 [0035]).

Consider claims 35 and 45, Philips further teaches signal processing unit further comprises: a supply circuit configured to supply a transmission digital signal to said radio unit through said second interface (page 3 [0035]), and said radio unit further comprises: a transmission signal converting circuit configured to generate said a transmission radio signal from said transmission digital signal supplied through said first and second interfaces (page 8 [0130]).

Consider claims 36 and 46, Philips further teaches supply circuit operates in response to said clock (page 3 [0038]).

Consider claims 37 and 47, Philips further teaches transmission signal converting circuit operates in response to said clock (page 3 [0035]).

Consider claims 38 and 48, Philips further teaches one of said first and second interfaces has a parallel bit converting function (page 9 [0142]).

***Allowable Subject Matter***

5. Claims 4-5 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any response to this action should be mailed to:

Mail Stop\_\_\_\_\_ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571)272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571)272-7882882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information Consider the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Nguyen  
Examiner  
Art Unit 2618

*TN*

*Quochien B. Vuong 01/07/08*

**QUOCHIEN B. VUONG  
PRIMARY EXAMINER**